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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,270	01/22/2002	Jae-Hyun Joo	9898-217	6757

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EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,270	JOO ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-15,17-20 and 24-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-15,17-20 and 24-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Status of the Claims

1. Amendment filed July 14, 2003 has been entered as Paper No. 10. Claim 21 has been canceled. Claims 7, 8, 20, 24 and 25-28 have been amended. Claims 1, 2, 4, 6-15, 17-20 and 24-32 are pending.

Response to Amendment

2. The amendment filed July 14, 2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "the crystallization annealing is lower than an *inherent temperature* of crystallization annealing of said capacitor dielectric layer" and "*the inherent crystallizing temperature of the tantalum oxide layer is over 700 ℃*".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 7,8, 24 and 25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitations "the crystallization annealing is lower than an *inherent temperature* of crystallization annealing of said capacitor dielectric layer" (claims 7, 18, 24 and 25) and "*the inherent crystallizing temperature of the tantalum oxide layer is over 700 ℃*" (claim 25) in the application as filed.

The specification does not provide support for any of the identified matters.

What is the inherent temperature of crystallization annealing of the capacitor dielectric layer ?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7, 18 and 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 7, lines 3-5 recites: "wherein the deposited capacitor dielectric layer has an **actual** crystallization annealing temperature that is lower than an **inherent** crystallization temperature of the dielectric layer".

First of all, "annealing temperature" is one of the process parameters that one chooses to perform. Some might choose a temperature (parameter) that is higher or lower than the other. Therefore, nothing is **inherent** about picking and choosing. It is only at one' own preference.

Secondly, inherent means the matter occurs 100 percent at all time. By Applicants' definition, the "inherent crystallization temperature of the dielectric layer" is the temperature that

the dielectric layer is crystallized. In this instant case, the "actual crystallization annealing temperature" is the temperature that Applicants performed to crystallize the dielectric layer.

The actual crystallization annealing temperature now becomes the inherent crystallization temperature of the dielectric layer.

Lines 7-8, recites: "subjecting the capacitor dielectric layer to a temperature that is lower than the *inherent* temperature of the dielectric layer until a crystallization annealing of the dielectric layer occurs".

A temperature can not be higher or lower than itself. Therefore, claim 7 is indefinite.

What temperature is the "inherent crystallization temperature of the dielectric layer" ?

How can an annealing temperature being lower than itself ?

Furthermore, the term "subjecting the capacitor dielectric layer to a temperature that is lower than the inherent temperature of the dielectric layer until a crystallization annealing of the dielectric layer occurs" is not understood.

Claims 18, 24 and 25 recite similar matter, thus, also indefinite.

With respect to claim 26-29, claims 26-29 recite the limitation "the selected atmosphere and the thermal annealing" in line 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claims 26-29 are indefinite therefore, a proper rejection on merit could not fairly provided.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 2, 4, 6-15, 17-20, 24, 25 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (U.S. Pub No. 2002/0037630) of record in view of Applicant admitted prior art.

With respect to claims 1 and 13, as best understood by the examiner, Agarwal teaches a method of fabricating a semiconductor device as claimed including:

forming a lower electrode (12) on a substrate (10) using a CVD process;

subjecting the lower electrode (12) to a pre-annealing, wherein the pre-annealing is a thermal annealing under a selected atmosphere;

forming a capacitor dielectric layer (28) on the pre-annealed lower electrode (12), wherein the capacitor dielectric layer (28) is formed of a crystallized material; and

forming an upper electrode (30) on the capacitor dielectric layer (28), wherein the lower electrode (12) is formed of metal. (See Figs. 1-7).

Thus, Agarwal is shown to teach all the features of the claim with the exception of explicitly disclosing the CVD process using a source having carbon.

However, the admitted prior art teaches that it is conventional in the art to form a lower electrode by a CVD process using a source having carbon.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the lower electrode (12) of Agarwal by a CVD process using a source having carbon as taught by the admitted prior art because the layer formed is more conformable to step differences of the underlaid structure. (See page 2, lines 10-16).

With respect to "subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode", Agarwal has subjected the lower electrode (12) to a pre-annealing, thus, the process of Agarwal, in view of admitted prior art, inherently results in removing carbon remaining in the lower electrode.

With respect to claims 2 and 14, the lower electrode (12) of Agarwal is formed of a material selected from the group consisting of a ruthenium.

With respect to claims 4 and 15, a metal organic material of the admitted prior art is used a source having carbon for the CVD method (MOCVD).

With respect to claims 6 and 17, the pre-annealing of Agarwal does not substantially change the materiality of the lower electrode (12).

With respect to claims 7 and 18, as best understood by the examiner, the step of forming a capacitor dielectric layer (28) of Agarwal includes:

depositing a capacitor dielectric layer on the pre-annealed lower electrode (12); and

after depositing the capacitor dielectric layer on the pre-annealed lower electrode (12) subjecting the capacitor dielectric layer (28) to a crystallization annealing temperature.

With respect to claims 8 and 31, the pre-annealing of Agarwal is performed at a temperature that overlaps the claimed range.

With respect to claims 9 and 19, the selected atmosphere or plasma atmosphere of Agarwal comprises hydrogen gas.

With respect to claim 10, the selected atmosphere of Agarwal comprises nitrogen gas.

With respect to claims 11 and 12, the selected atmosphere of Agarwal is a mixed atmosphere comprises hydrogen and nitrogen.

With respect to claims 30 and 32, Agarwal teaches subjecting the metal lower electrode (12) to a pre-annealing in selected atmosphere comprises hydrogen gas (reducing ambient) at a temperature that higher than the claimed range. The claimed temperature range does not appear to be critical.

However, Agarwal also teaches that the temperature required for the pre-annealing process may be reduced if reducing ambient is used.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to reduce the pre-annealing temperature of Agarwal since the reducing ambient is used.

Further, within purview of one having ordinary skill in the art at the time of invention, it would have been obvious to determine the optimum pre-annealing temperature in reducing

ambient to treat the lower electrode. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

With respect to claim 20, as best understood by the examiner, Agarwal teaches a method of fabricating a semiconductor device as claimed including:

forming a lower electrode (12) on a substrate (10), by a CVD method;

subjecting the lower electrode (12) to a pre-annealing, wherein the pre-annealing is a treatment exposing the lower electrode under plasma atmosphere;

depositing a tantalum oxide layer (28) on the pre-annealed lower electrode (12);

crystallizing the tantalum oxide layer (28) at a crystallizing temperature; and

forming an upper electrode (30) on the capacitor dielectric layer (28), wherein the lower electrode is formed of metal, the pre-annealing is performed at a range of temperature, and the materiality and surface morphology of the lower electrode does not substantially change by the pre-annealing.. (See Figs. 1-7).

With respect to a CVD method using source having carbon, a similar reason as that of claims 1 and 13 is also applied here.

With respect to the pre-annealing temperature, the pre-annealing temperature of Agarwal is overlapped the claimed range.

With respect to "subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode" a similar reason as that of claims 1 and 13 is also applied here.

With respect to claim 24, as best understood by the examiner, the temperature of Agarwal is the crystallization temperature.

With respect to claim 25, as best understood by the examiner, the tantalum oxide layer (28) of Agarwal is crystallized at a temperature (600-800 °C) that includes the claimed range (650 °C).

Response to Arguments

6. Applicant's arguments filed July 14, 2003 have been fully considered but they are not persuasive.

Rejection under 35 USC § 112

With respect to claims 7, 8, 24 and 25, Applicants argument with respect to "inherent temperature" is not a fact. Applicants fail to provide support for his contention.

With respect to claim 25, at best, page 2, lines 23-24 state: "The capacitor dielectric layer is then subjected to a crystallization annealing which is performed at 700 °C".

This temperature is not an "inherent temperature". It is just a temperature used by a prior art. "Inherent" means must be performed or no crystallization will take place. The present pre-annealing temperature is conducted at lower than that temperature, 700 °C, and crystallization occurs. Therefore, nothing is inherent about "700 °C". It is just a preference.

Rejection under 35 USC § 103

With respect to claims 1 and 13, Applicants appear to contend that the dielectric layer of Agarwal is not a crystallized dielectric and cited paragraph [0048] to support his contention.

However, Agarwal *implicitly* refers to a crystallized dielectric layer in paragraph [0055]: "In a completed capacitor, the anneal process tends to *increase capacitance* by about 20% with respect to a capacitor without annealing and to reduce leakage current".

Further, in [0057] Agarwal teaches: "after the dielectric layer and the electrode layers are formed, the capacitor is annealed as described above".

One should ask why an annealed capacitor has higher capacitance than the one without annealed and what has happened in the dielectric layer that leakage current is reduced.

Applicants have acknowledged the increase in capacitance is a direct result of crystallizing the dielectric layer in page 2, lines 23-25 "The capacitor dielectric layer is then subjected to a crystallization annealing which is performed at 700 °C for 30 minutes in a nitrogen atmosphere in ORDER TO INCREASE THE CAPACITANCE of the capacitor".

Applicant further add: "It would not be obvious to use the CVD process using a source having carbon with Agarwal process because of the inherent disadvantages.

However, Applicant recognized that the disadvantage only occurs if the lower electrode is not subjected to a pre-annealing process.

In the instant case, said disadvantage is a non-issue because, the lower electrode of Agarwal has been subjected to a pre-anneal process. Therefore, contaminants, such as carbon, if remained following the deposit should out diffuse when the pre-anneal is performed.

With respect to claim 20, contrary to Applicant assertion, the pre-annealing of Agarwal DOES NOT SUBSTANTIALLY change the materiality of the lower electrode. Since the lower

electrode of Agarwal may have both ruthenium and ruthenium oxide ([0014]) therefore, converts at least some of the ruthenium oxide to ruthenium ([0015]) DOES NOT SUBSTANTIALLY change the material of the lower electrode.

The rejections are therefore, maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
September 3, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800